

**ABSTRACT**

A capping layer (118) is used during an anneal to form fully silicided NiSi gate electrodes (120). The capping layer (118) comprises a material with an affinity for boron, such as TiN. The capping layer (118) serves as a boron trap that reduces the interface boron concentration for PMOS transistors without reducing the interface arsenic concentration for NMOS transistors.